CLAIMS

What is claimed is:

1. A method for producing a reduced bounding box for a net in a VLSI design of cells, where at least one cell in the design includes two or more pins by which the cell can be connected to at least one other cell in the design, the method comprising:

creating a set of electronic records configured to store information about one or more pins and one or more ports connected to the net in the design;

storing data about the one or more pins in one or more data structures configured to store pin data, where the data about the one or more pins facilitates relating the one or more pins to one or more electronic records in the set of electronic records;

selectively arranging the set of electronic records in a pre-determined order;

producing an initial bounding box for the net in the design;

analyzing the selectively arranged set of electronic records to identify a corner case of pins in the initial bounding box;

selectively removing pins in a corner case of pins to produce an intermediate bounding box from the initial bounding box;

reducing the size of the intermediate bounding box by repetitively selectively removing one or more pins from inclusion in the intermediate bounding box; and

producing the reduced bounding box by further reducing the size of the intermediate bounding box by repetitively selectively moving an edge of the intermediate bounding box.

2. The method of claim 1, where an electronic record in the set of electronic records includes one or more of, an (x,y) position of a pin in the design, the port in which the pin is located, an indicator concerning whether the pin is a candidate to be included in the reduced bounding box, an indicator concerning whether the pin has been logically excluded from the reduced bounding box, and an indicator concerning whether a pin is currently on an edge of an intermediate bounding box.

3. The method of claim 1, where an electronic record in the set of electronic records comprises an entry in a table.

4. The method of claim 1, where an electronic record in the set of electronic records comprises a set of related entries in a set of related data structures.

5. The method of claim 1, where an electronic record in the set of electronic records comprises a set of related entries in a set of related arrays.

6. The method of claim 1, where the pin data comprises one or more of, a pin identifier, and a pointer to a pin.

7. The method of claim 1, where the data structures configured to store pin data comprise one or more arrays.

8. The method of claim 7, comprising a first data structure configured to store pin data in order by x position.

9. The method of claim 8, comprising a second data structure configured to store pin data in order by y position.

10. The method of claim 9, where selectively arranging the set of electronic records includes:

sorting the pin data in the first data structure in order by x position; and

sorting the pin data in the second data structure in order by y position.

11. The method of claim 1, where the pre-determined order to which the set of electronic records is arranged facilitates one or more of, identifying a corner case, identifying a pin that is a candidate for removal from the intermediate bounding box, and identifying an edge in the intermediate bounding box that is a candidate to be moved.

12. The method of claim 1, where identifying a corner case of pins comprises:

identifying that two or more pins in a corner of the initial bounding box are in the same port;

determining that the port has more than one pin; and

determining that the port does not have pins on opposite edges of the initial bounding box.

13. The method of claim 10, where selectively removing pins in the corner case of pins comprises:

computing the Manhattan distance from one or more pins in the first data structure to the corner of the design in which the pins are located;

selecting the pin in the first data structure with the greatest Manhattan distance to the corner; and

selectively excluding pins from the first data structure that are not the pin in the first data structure with the greatest Manhattan distance.

14. The method of claim 13, where selectively removing pins in the corner case of pins comprises:

computing the Manhattan distance from one or more pins in the second data structure to the second corner of the design in which the pins are located;

selecting the pin in the second data structure with the greatest Manhattan distance to the second corner; and

selectively excluding pins from the second data structure that are not the pin in the second data structure with the greatest Manhattan distance.

15. The method of claim 1, where reducing the size of the intermediate bounding box by repetitively selectively removing one or more pins from inclusion in the intermediate bounding box and repetitively, selectively moving an edge of the intermediate bounding box comprises:

creating a four element edge array;

storing edge and pointer data in the four element edge array;

arranging the edge and pointer data in the edge array to facilitate determining which edge of the intermediate bounding box to move; and

selectively moving an edge of the intermediate bounding box based on the data in the four element edge array.

16. The method of claim 1, where the reduced bounding box comprises the minimal bounding box for the net in the design.

17. A computer-readable medium storing processor executable instructions operable to perform a method for producing a reduced bounding box for a net in a VLSI design of cells, where at least one cell in the design includes two or more pins by which the cell can be connected to at least one other cell in the design, the method comprising:

creating a set of electronic records configured to store information about one or more pins and one or more ports connected to the net in a design for which the reduced bounding box is to be produced;

storing data about the one or more pins in one or more data structures configured to store pin data, where the data about the one or more pins facilitates relating the one or more pins to one or more electronic records in the set of electronic records;

selectively arranging the set of electronic records in a pre-determined order;

producing an initial bounding box for the net in the design;

analyzing the selectively arranged set of electronic records to identify a corner case of pins in the initial bounding box;

selectively removing pins in a corner case of pins to produce an intermediate bounding box from the initial bounding box;

reducing the size of the intermediate bounding box by repetitively selectively removing one or more pins from inclusion in the intermediate bounding box; and

producing the reduced bounding box by further reducing the size of the intermediate bounding box by repetitively selectively moving an edge of the intermediate bounding box.

18. A method for computing a reduced bounding box for a net in a VLSI design of cells, comprising:

receiving a VLSI design of cells where at least one cell in the VLSI design of cells includes more than one pin by which it can be connected to at least one other cell in the design;

producing an initial bounding box for the net in the design; and

computing the reduced bounding box by reducing the initial bounding box.

19. The method of claim 18, where reducing the initial bounding box comprises:

selectively repetitively producing a intermediate bounding box that is smaller than the initial bounding box by:

selectively re-establishing one or more corner pins in the intermediate bounding box when there are two or more pins in a port in a corner of the intermediate bounding box, when the port has more than one pin, and when the port does not have pins on opposite edges of the intermediate bounding box; and

selectively moving one or more edges of the intermediate bounding box.

20. The method of claim 18, comprising:

displaying the reduced bounding box.

21. The method of claim 18, comprising:

selectively generating a signal associated with the reduced bounding box.

22. The method of claim 18, where the reduced bounding box is a minimal bounding box for the net in the design.

23. A computer-readable medium storing processor executable instructions operable to perform a method for computing a reduced bounding box for a net in a VLSI design of cells, comprising:

receiving a VLSI design of cells where at least one cell in the VLSI design of cells includes more than one pin by which it can be connected to at least one other cell in the design;

producing an initial bounding box for the net in the design; and

computing the reduced bounding box by reducing the initial bounding box.

24. A system, comprising:

a bounding box memory configured to store design data associated with a net in a design for which a bounding box is to be reduced, where at least one cell in the design includes two or more pins by which it can be connected to at least one other cell in the design; and

a reducing logic operably connected to the bounding box memory, where the reducing logic is configured to compute a reduced bounding box.

25. The system of claim 24, where the reducing logic is configured to:

receive the design;

produce an initial bounding box for a net in the design; and

reduce the bounding box for the net in the design by:

selectively re-establishing one or more corner pins in the bounding box when there are two or more pins in the same port in a corner of the bounding box, when the port has more than one pin, and when the port does not have pins on opposite edges of the bounding box; and

selectively moving one or more edges of the bounding box.

26. The system of claim 25, comprising:

a display configured to display the reduced bounding box.

27. The system of claim 24, where the reduced bounding box is the minimal bounding box for the net in the design.

28. The system of claim 24, comprising:

a design receiving logic configured to receive the design;

an initial bounding box logic configured to produce the initial bounding box for a net in the design; and

a corner case logic configured to identify or remove pins from a corner case of pins.

29. A system for producing a minimal bounding box for a net in a VLSI design of cells, where one or more cells may include two or more pins by which the one or more cells can be connected to one or more other cells, the system comprising:

means for receiving a VLSI design of cells;

means for producing an initial bounding box;

means for identifying pins in corners that may be excluded; and

means for moving edges in the bounding box.